

Automatic



Washing Machine



Control System



Using Verilog HDL

**INTRODUCTION**

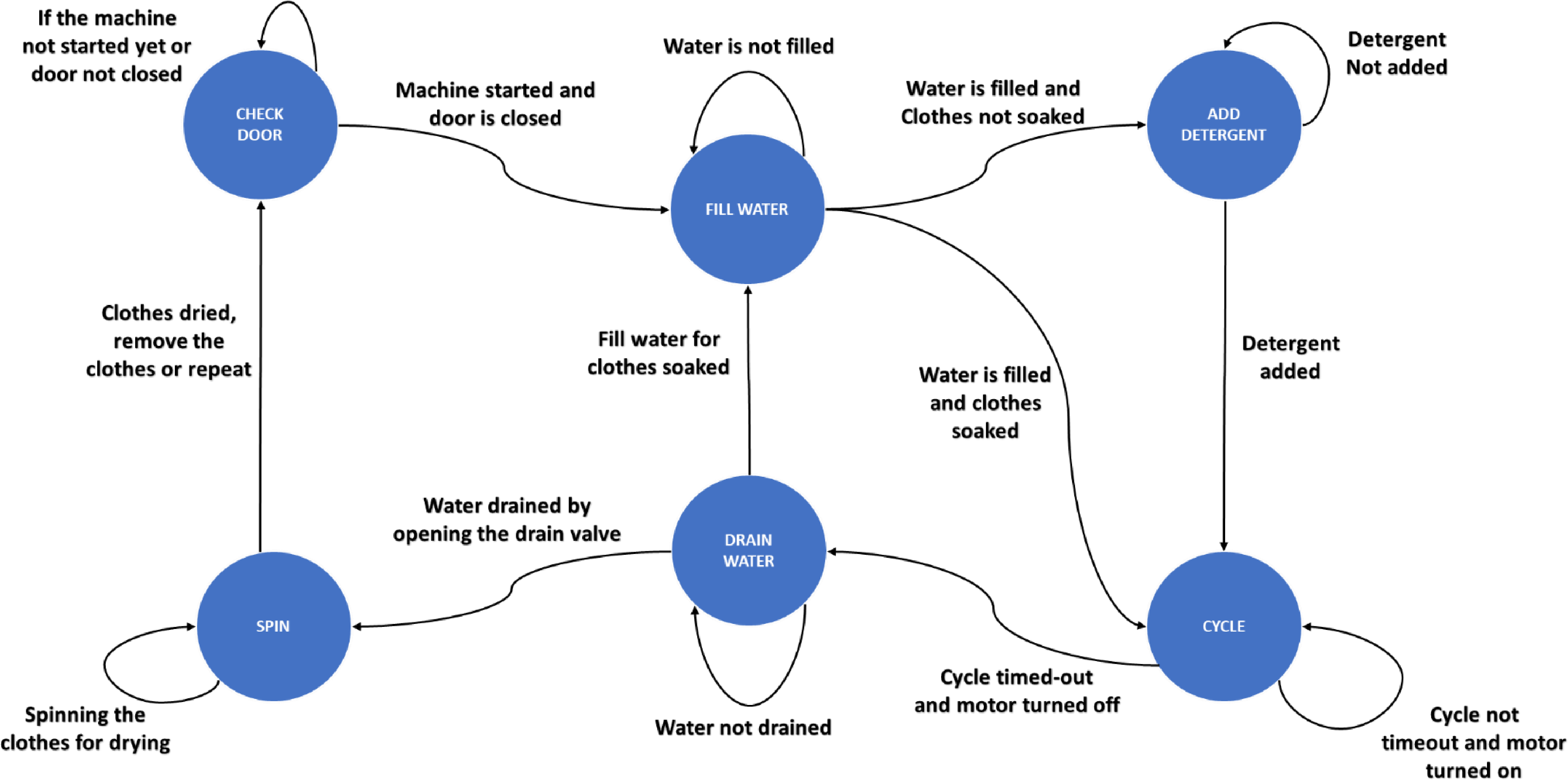
Various real life scenarios can be represented by Finite State Machines like control system of an automatic washing machine.

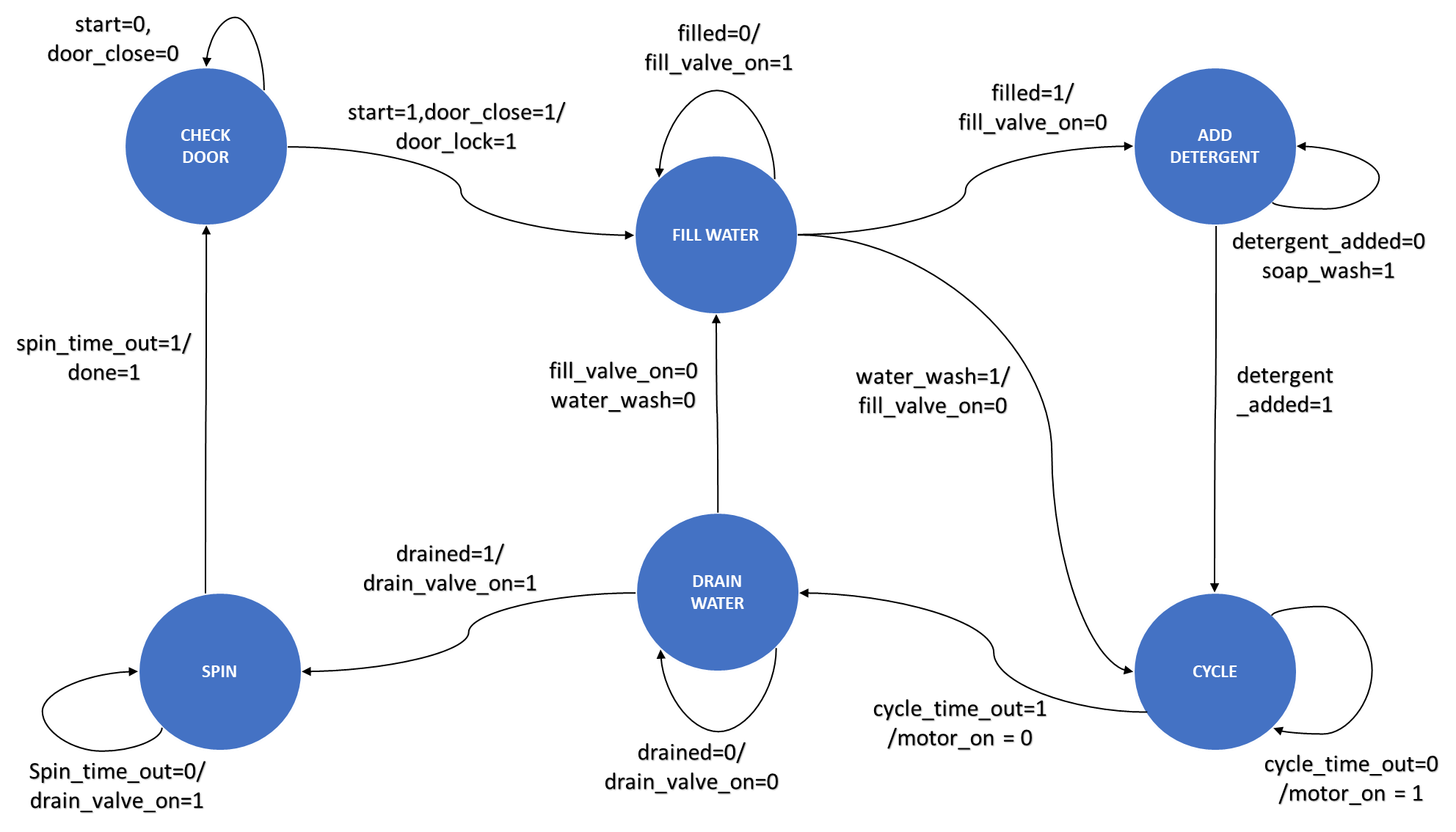
Assigning the main stages of the process like Close door, fill water, add detergent, cycle, drain and spin various states that can be implemented as a State Machine.

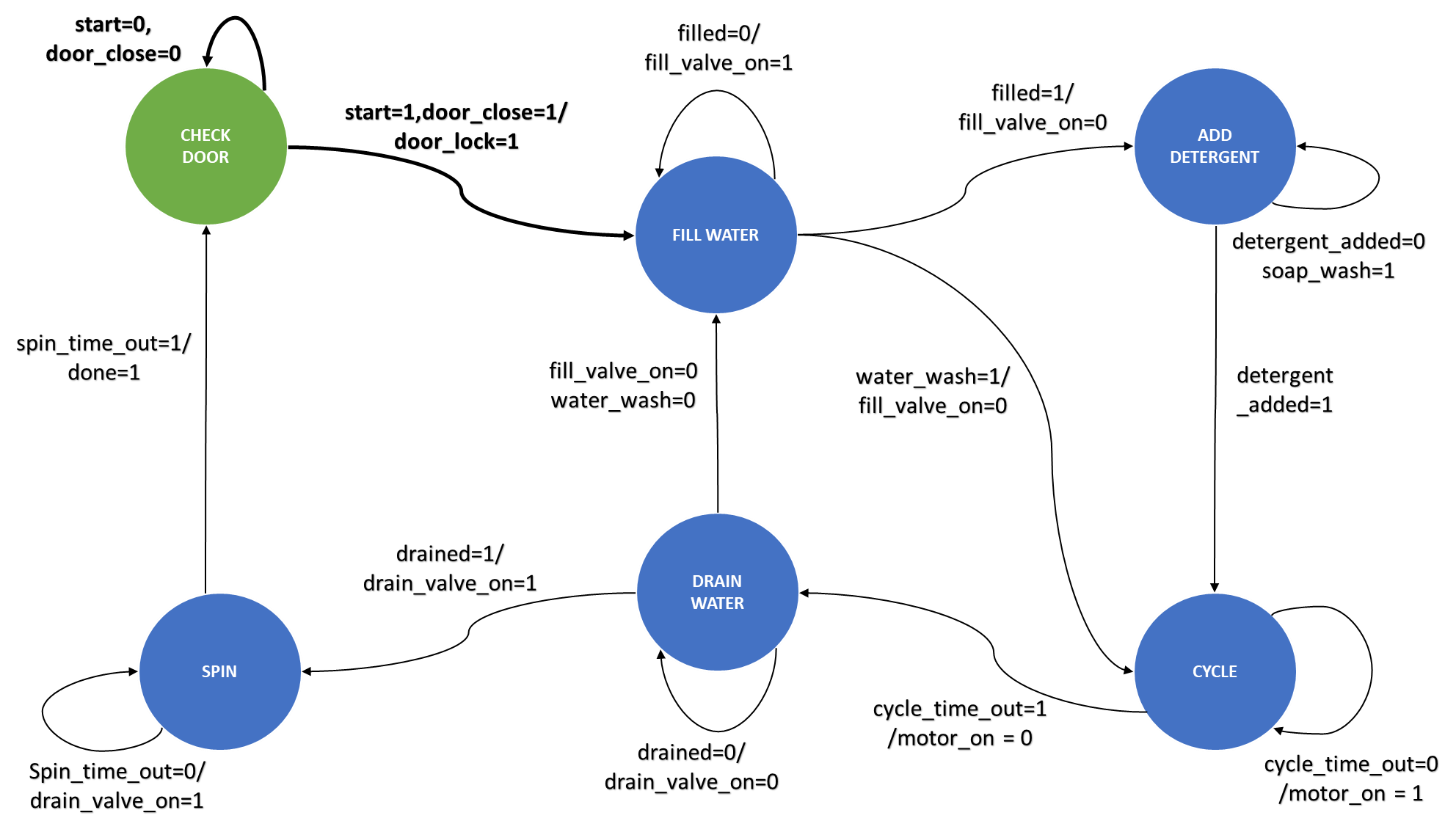
Writing a test bench to observe the working of the machine.

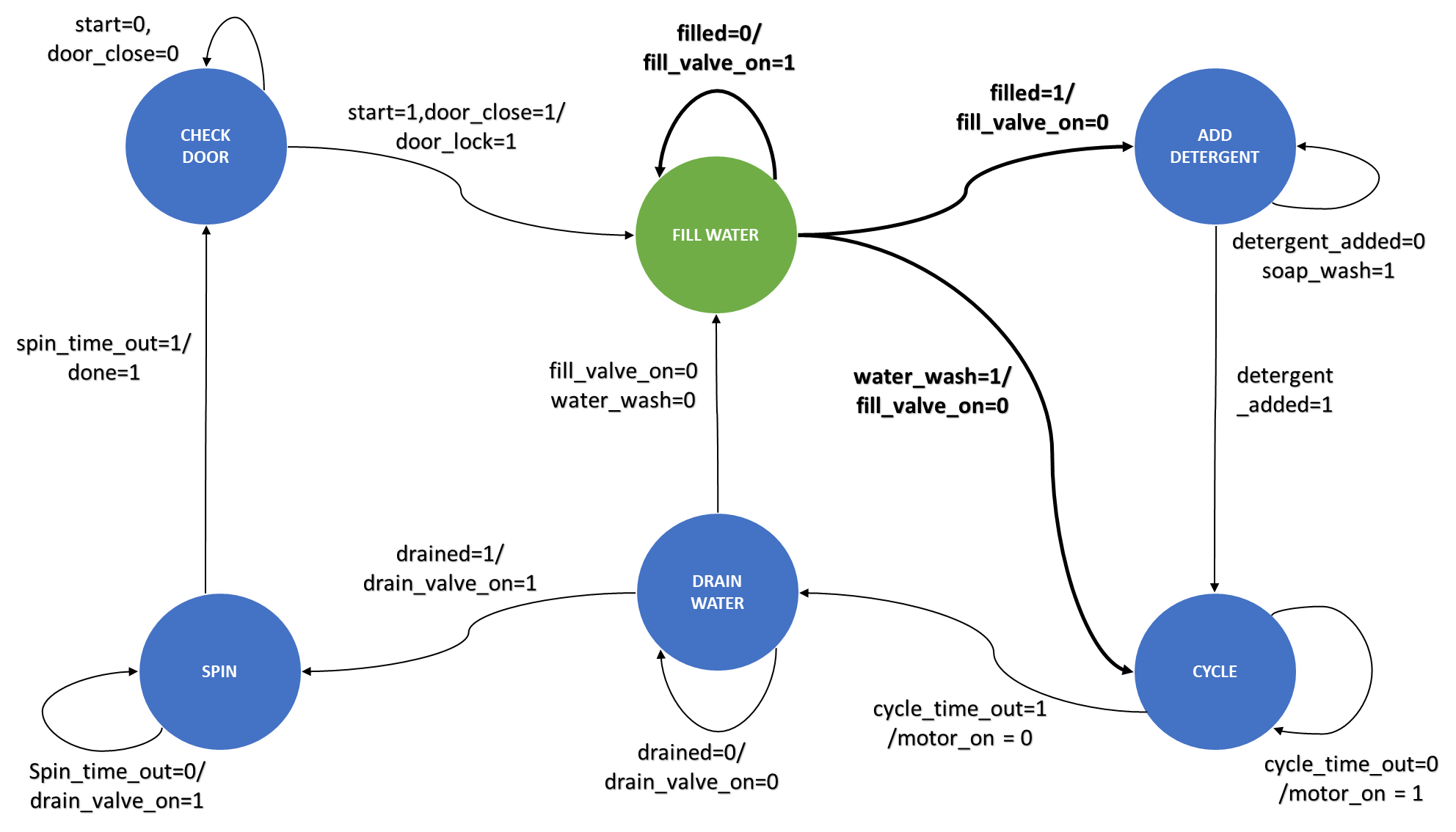
Using Xilinx ISE 14.7 to implement the control system.

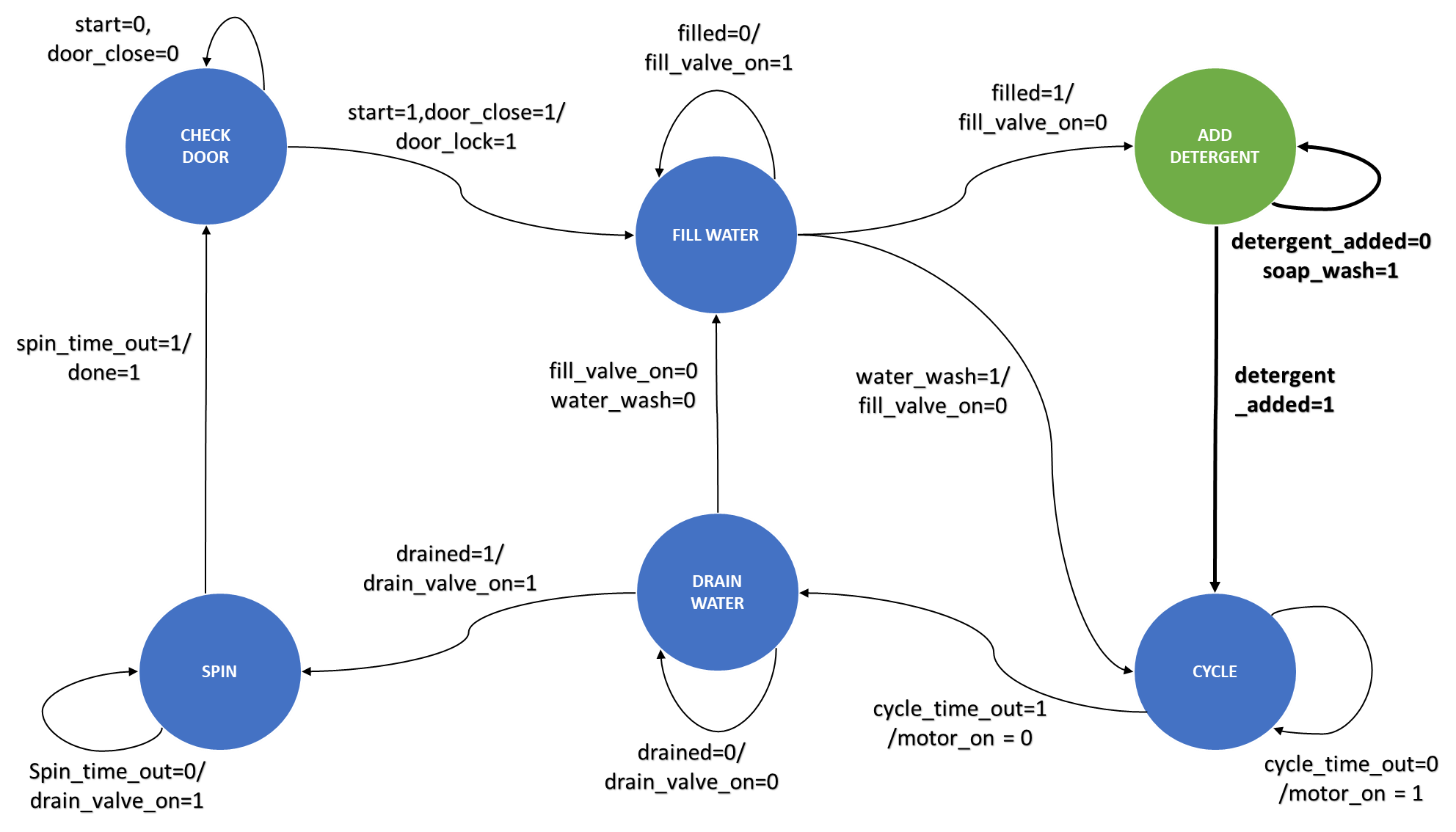
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| **STATE DIAGRAM** |

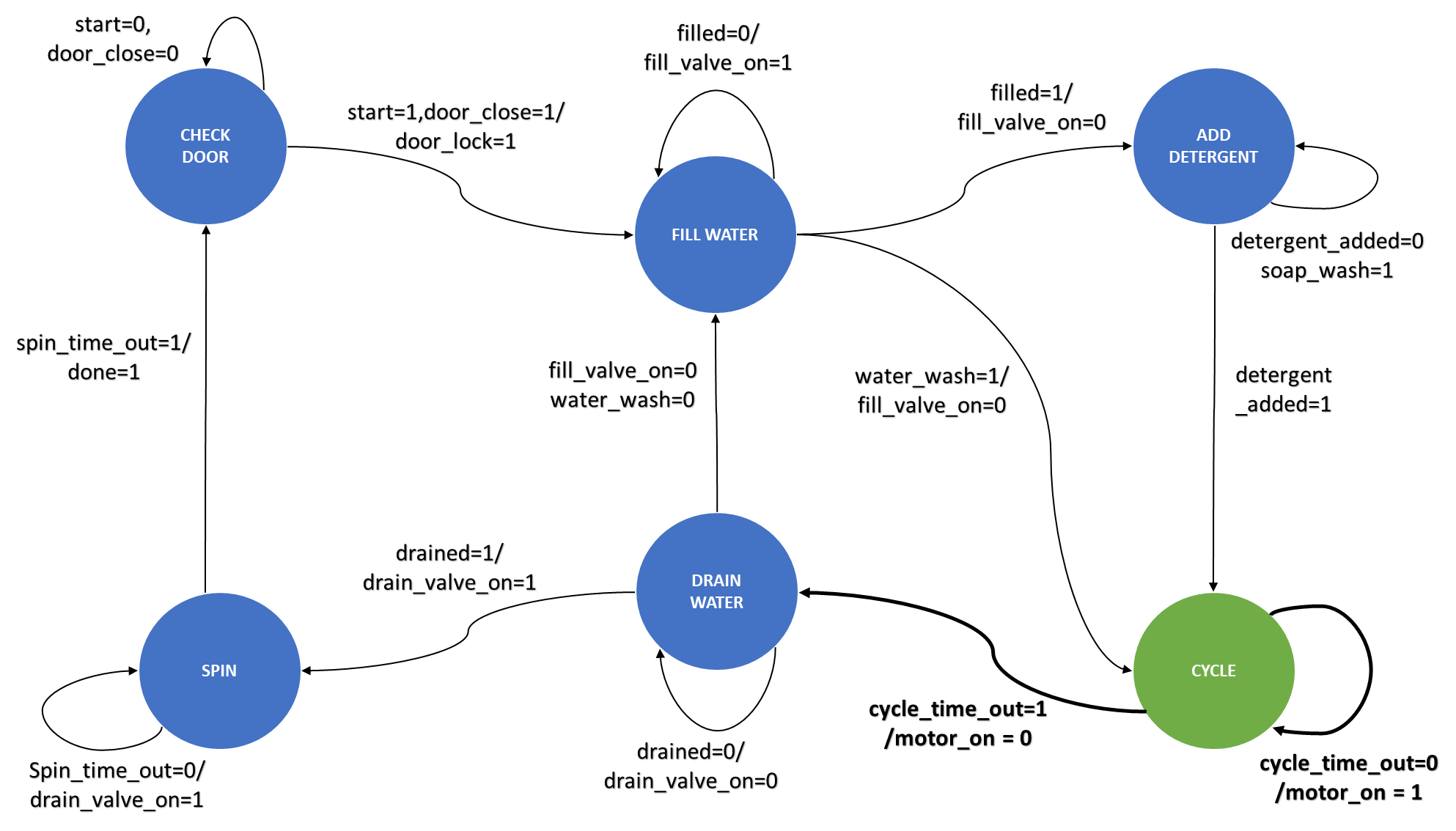


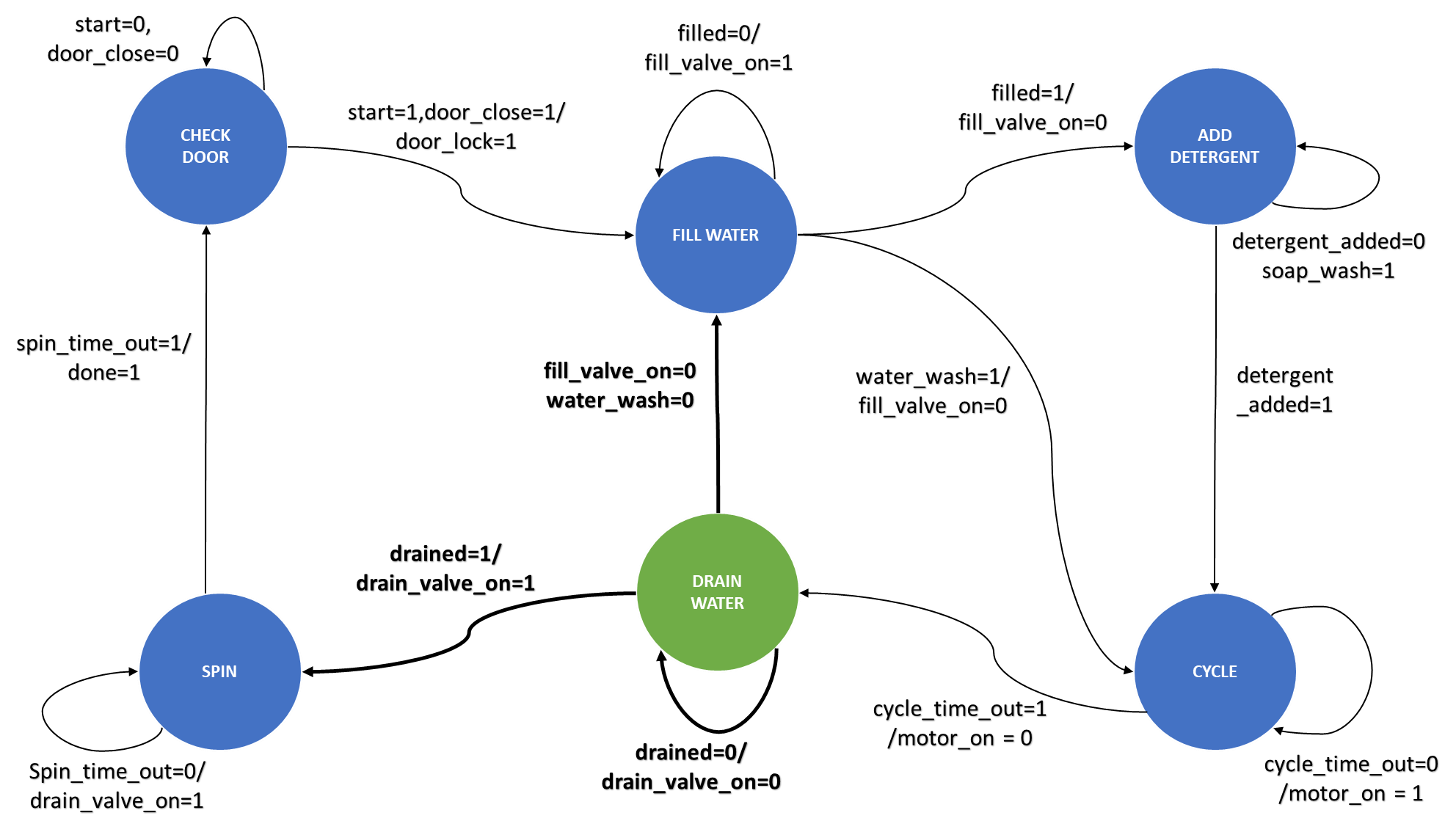


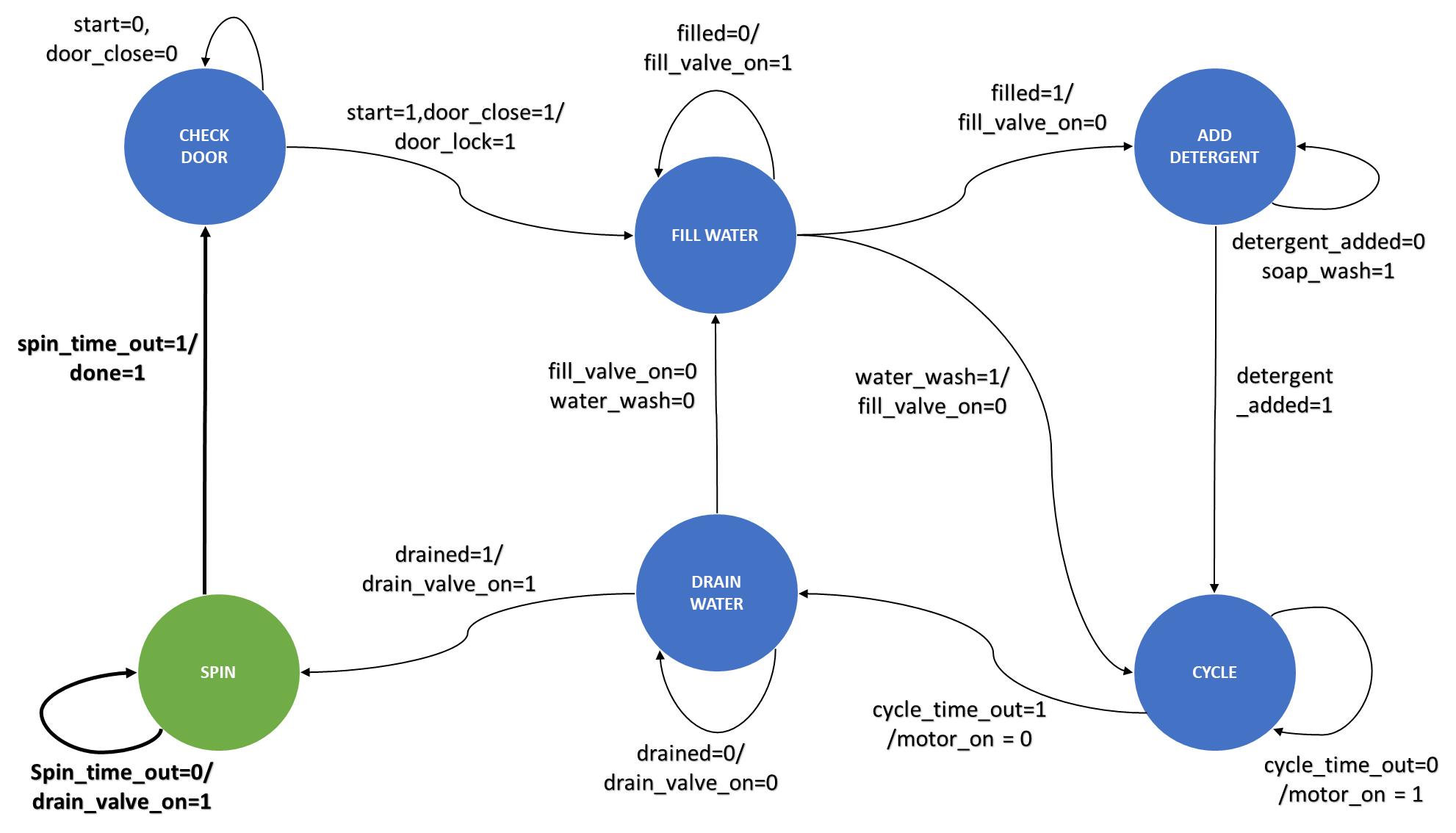












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| **RESULTS** |

# FUTURE SCOPE AND APPLICATIONS

4

3

2

1

The current project can be implemented on FPGA to demonstrate the code.

The automatic washing machine has been implemented on Verilog

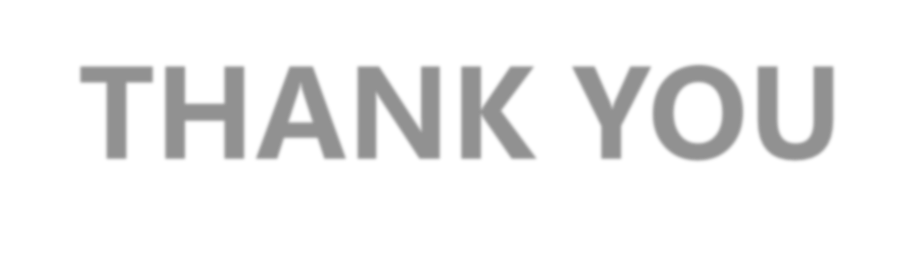
HDL using Xilinx ISE.

The project is based on Finite State Machine (FSM). Various other projects based on FSM can

be implemented using the current project code as the basis.

More functionality may be included like different modes to wash the clothes based on the clothing material,

temperature etc

**THANK YOU**

**Mail Id: vadthyavath22bec56@iiitkottayam.ac.in**